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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,854	12/22/2000	James Morrow	10407/476	7292

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EXAMINER	
PATEL, NIKETA I	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,854	MORROW ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

2. Applicant's arguments, see pages 7-10, filed 10/11/2005, with respect to the rejection(s) of claim(s) 1-34 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Nair et al. U.S. Patent Number: 6,675,226 B1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6-20, 22-27, 29-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Nair et al. U.S. Patent Number: 6,675,226 B1 (hereinafter "*Nair*".)

1. **Referring to claims 1, 12, 19, 24**, *Nair* teaches a generic device controller unit system and a method for facilitating interaction between a processor and any number of peripheral devices [see abstract], the system comprising: a general purpose device controller employing

asynchronous true real time peripheral device control [see column 2, lines 16-40 and column 11, lines 14-45 and figure 2, element 43], wherein the device controller interfaces between a non-true real time operating system and the peripheral devices [see column 2, lines 16-40 and column 4, lines 14-35 and figure 2, elements 12, 42, A, B, C, D, E, F], thereby allowing a non-true real time operating system to implement true real time control of the peripheral devices [see column 2, lines 16-40 and column 4, lines 14-35]; and a data and protocol communications interface, wherein the communications interface connects the processor and the peripheral devices [see column 2, lines 16-40 and column 4, lines 14-35], thereby allowing the processor to utilize a single protocol and associated data to communicate with the peripheral devices which may be utilizing protocols and associated data which are different than that used by the processor [see column 2, lines 16-40 and column 4, lines 14-35.]

2. **Referring to claims 3, 14, 20, 26**, *Nair* teaches the system and the method wherein the generic device controller unit system functions as a distributed processing environment [see column 4, lines 57-63.]

3. **Referring to claims 4, 27**, *Nair* teaches the system and the method wherein the generic device controller unit system further includes customized system drivers [see column 5, lines 55-62 and figure 2, elements 43, 45.]

4. **Referring to claims 6, 18, 29**, *Nair* teaches the system and the method wherein the generic device controller unit system interfaces with the non-true real time operating system that functions in a Win32 environment [see column 4, lines 14-21, 'Windows NT'.]

5. **Referring to claims 7, 15, 22, 30**, *Nair* teaches the system and the method wherein the generic device controller unit system is an input/output device interface for a processor to peripheral devices [figure 2, elements 34, 43, 45, 12, 42, A, B, C, D, E, F.]

6. **Referring to claims 8, 16, 31**, *Nair* teaches the system and the method wherein the generic device controller unit system provides real time device control to resource management capabilities of a standard non-true real time operating system [see abstract.]

7. **Referring to claims 9, 17, 23, 32**, *Nair* teaches the system and the method wherein the generic device controller unit system produces true real time peripheral device control without the higher level functionality of the processor [see column 2, lines 16-40 and column 4, lines 14-35.]

8. **Referring to claims 10, 33**, *Nair* teaches the system and the method wherein the generic device controller unit system produces true real time peripheral device control without the processor using a true real time kernel [see column 2, lines 16-40 and column 4, lines 14-35.]

9. **Referring to claims 11, 34**, *Nair* teaches the system and the method wherein the generic device controller unit system produces true real time peripheral device control without the processor utilizing a layered true real time operating system [see column 2, lines 16-40 and column 4, lines 14-35.]

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 21, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair et al. U.S. Patent Number: 6,675,226 B1 (hereinafter "*Nair*") and further in view of Microsoft Computer Dictionary, page 543 (hereinafter "*MCD*".)

11. **Referring to claims 5, 21, 28**, teachings of *Nair* as modified by the teachings of teaches a generic device controller unit system and a method for facilitating interaction between a processor and any number of peripheral devices [see abstract.] *Nair* does not set forth the limitation wherein Universal Serial Bus is the default communication protocol between the generic device controller unit system and the processor, however *MCD* teaches that USB is well known type of bus used with a computer system because it supports the ability to automatically add and configure new devices and the ability to add such devices without having to shut down and restart the system.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of being able to connect up to 127 peripherals to a processor by using Universal Serial Bus. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include Universal Serial Bus to get this advantage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272 4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
10/27/2005

10/28/05

HENRY W. H. TSAI
PRIMARY EXAMINER